L Number	Hits	Search Text	DB	Time stamp
7	31	(covering with beak) and (field adj oxide)	USPAT; US-PGPUB	2004/08/31 08:59
8	589	(covering with (field adj oxide))	USPAT; US-PGPUB	2004/08/31 09:00
9	580	((covering with (field adj oxide))) not ((covering with beak) and (field adj oxide))	USPAT; US-PGPUB	2004/08/31 09:00
10	555	(((covering with (field adj oxide))) not ((covering with beak) and (field adj oxide))) and @ad<20020719	USPAT; US-PGPUB	2004/08/31 11:07
11	81	((((covering with (field adj oxide))) not ((covering with beak) and (field adj oxide))) and @ad<20020719) and clean$3	USPAT; US-PGPUB	2004/08/31 09:55
12	0	(covering with STI) and MISFET	USPAT; US-PGPUB	2004/08/31 09:56
13	0	(protecting with STI) and MISFET	USPAT; US-PGPUB	2004/08/31 09:56
14	1	(protect with STI) and MISFET	USPAT; US-PGPUB	2004/08/31 09:57
15	0	(protect with STI) and MISFET	EPO; JPO; DERWENT; IBM_TDB	2004/08/31 09:57
16	0	(protecting with STI) and MISFET	EPO; JPO; DERWENT; IBM_TDB	2004/08/31 09:58
17	0	(covering same STI) and MISFET	EPO; JPO; DERWENT; IBM_TDB	2004/08/31 09:58
18	0	(protecting same STI) and MISFET	EPO; JPO; DERWENT; IBM_TDB	2004/08/31 09:58
19	0	(protecting same STI) and MOSFET	EPO; JPO; DERWENT; IBM_TDB	2004/08/31 09:58
20	0	(covering same STI) and MOSFET	EPO; JPO; DERWENT; IBM_TDB	2004/08/31 09:59
21	44	(covering same STI) and MOSFET	USPAT; US-PGPUB	2004/08/31 09:59
22	37	((covering same STI) and MOSFET) and @ad<20020719	USPAT; US-PGPUB	2004/08/31 10:02
23	71	MISFET and STI and @ad<20020719	USPAT; US-PGPUB	2004/08/31 10:17
24	14	(MISFET and STI and @ad<20020719) and cleaning	USPAT; US-PGPUB	2004/08/31 10:05
25	6	(MISFET and STI and @ad<20020719) and clean	USPAT; US-PGPUB	2004/08/31 10:05
26	2	((MISFET and STI and @ad<20020719) and clean) not ((MISFET and STI and @ad<20020719) and cleaning)	USPAT; US-PGPUB	2004/08/31 10:13
27	69	(MISFET and STI and @ad<20020719) and etching	USPAT; US-PGPUB	2004/08/31 10:05
28	55	((MISFET and STI and @ad<20020719) and etching) not ((MISFET and STI and @ad<20020719) and cleaning)	USPAT; US-PGPUB	2004/08/31 10:06
29	5	((((covering with (field adj oxide))) not ((covering with beak) and (field adj oxide))) and @ad<20020719) and MISFET	USPAT; US-PGPUB	2004/08/31 11:07
30	57	(MISFET and STI and @ad<20020719) not ((MISFET and STI and @ad<20020719) and cleaning)	USPAT; US-PGPUB	2004/08/31 10:13
31	1	MISFET and STI	EPO; JPO; DERWENT; IBM_TDB	2004/08/31 10:17
32	0	MISFET and (FOX with STI) and @ad<20020719	USPAT; US-PGPUB	2004/08/31 11:07
33	5	MISFET and ((field adj oxide) with STI) and @ad<20020719	USPAT; US-PGPUB	2004/08/31 11:07

US-PAT-NO: 6411548

DOCUMENT-IDENTIFIER: US 6411548 B1

TITLE: Semiconductor memory having transistors connected in series

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Detailed Description Text - DETX (176):
First of all, as shown in FIG. 29, an n-type impurity is implanted into the p-type silicon substrate 21 by the ion implantation method to form the n-type well region 22. In addition, a p-type impurity is implanted into the n-type well region 22 to form the p-type well region 23. Element isolation layers linearly extending in the column direction are formed on the silicon substrate 21. The element isolation layers may be **field oxide** films formed by the LOCOS method or layers having an **STI** (Shallow Trench Isolation) structure.